AMENDMENT TO CLAIMS

1-11. (Cancelled)

12. (Currently Amended) A method for fabricating a semiconductor device, the method comprising the steps of:

forming a conductive film on a specified region of a substrate;

forming an insulating film on the substrate such that the conductive film is covered with the insulating film;

forming, on the insulating film, a mask layer having a first opening pattern above the conductive film;

performing first etching with respect to the insulating film by using the mask layer having the first opening pattern to form, in the insulating film, a depressed portion having a bottom portion not reaching the conductive film;

forming a mask layer having a second opening pattern having an opening diameter larger than an opening diameter of the first opening pattern by enlarging the opening diameter of the first opening pattern; and

performing second etching with respect to the insulating film by using the mask layer having the second opening pattern to form, in the insulating film, an opening for exposing the conductive film ~~such that the opening has a diameter larger than a diameter of the depressed portion and a wall surface having a tapered configuration,~~

wherein a diameter of the opening increases gradually from the bottom portion toward the top portion.

13. (Original) The method of claim 12, further comprising the step of:

forming, at least in the opening, a capacitor element composed of a lower electrode, a capacitor insulating film, and an upper electrode.

14. (Original) The method of claim 13, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode;

forming the capacitor insulating film on the lower electrode; and

forming the upper electrode on the capacitor insulating film.

15. (Previously presented) The method of claim 12, further comprising, between the step of forming the mask layer having the first opening pattern and the step of forming the depressed portion in the insulating film, the step of:

forming a wall surface of the first opening pattern into a tapered configuration.

16. (Previously presented) The method of claim 12, further comprising, after the step of forming the opening in the insulating film, the step of:

after removing the mask layer, performing third etching with respect to an entire surface of the insulating film to smooth the tapered configuration of the wall surface of the opening.

17. (Previously presented) The method of claim 12, further comprising, after the step of forming the opening in the insulating film, the steps of:

forming a mask layer having a third opening pattern having an opening diameter larger than the opening diameter of the second opening pattern by enlarging the opening diameter of the second opening pattern; and

performing third etching with respect to the insulating film by using the mask layer having the third opening pattern to smooth the tapered configuration of the wall surface of the opening.

18. (Previously presented) The method of claim 16, further comprising, after the step of smoothing the tapered configuration of the wall surface of the opening, the step of:

forming, at least in the opening, a capacitor element composed of a lower electrode, a capacitor insulating film, and an upper electrode.

19. (Original) The method of claim 18, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode;

forming the capacitor insulating film on the lower electrode; and

forming the upper electrode on the capacitor insulating film.

20. (Previously presented) A method for fabricating a semiconductor device, the method comprising the steps of:

forming a conductive film on a specified region of a substrate;

forming an etching stopper film on the conductive film;

forming an insulating film on the substrate such that the etching stopper film is covered with the insulating film;

forming, on the insulating film, a mask layer having a first opening pattern above the conductive film;

performing first etching with respect to the insulating film by using the mask layer having the first opening pattern to form, in the insulating film, a depressed portion having a bottom portion not reaching the etching stopper film;

forming a mask layer having a second opening pattern having an opening diameter larger than an opening diameter of the first opening pattern by enlarging the opening diameter of the first opening pattern;

performing second etching with respect to the insulating film by using the mask layer having the second opening pattern to form, in the insulating film, an opening for exposing the etching stopper film such that the opening has a diameter larger than a diameter of the depressed portion and a wall surface having a tapered configuration; and

performing third etching with respect to the etching stopper film and thereby form, in the etching stopper film, an opening for exposing the conductive film, while smoothing the tapered configuration of the wall surface of the opening of the insulating film.

21. (Original) The method of claim 20, further comprising the step of:

forming a capacitor element composed of a lower electrode, a capacitor insulating film, and an upper electrode at least in the opening of the insulating film and in the opening of the etching stopper film.

22. (Original) The method of claim 21, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode;

forming the capacitor insulating film on the lower electrode; and

forming the upper electrode on the capacitor insulating film.

23. (Previously presented) The method of claim 20, wherein the third etching is performed after removing the mask layer.

24. (Previously presented) The method of claim 20, wherein the third etching is performed by using a mask layer having a third opening pattern formed by enlarging the opening diameter of the second opening pattern.

25. (Previously presented) The method of claim 20, further comprising, between the step of forming the mask layer having the first opening pattern and the step of forming the depressed portion in the insulating film, the step of:

forming a wall surface of the first opening pattern into a tapered configuration.

26. (Original) The method of claim 20, wherein the etching stopper film is composed of a metal oxide containing titanium or aluminum.

27. (Previously presented) A method for fabricating a semiconductor device, the method comprising the steps of:

forming a conductive film on a specified region of a substrate;

forming an insulating film on the substrate such that the conductive film is covered with the insulating film;

forming, on the insulating film, a mask layer having a first opening pattern above the conductive film;

performing first etching with respect to the insulating film by using the mask layer having the first opening pattern to form, in the insulating film, a depressed portion having a bottom portion not reaching the conductive film; and,

after removing the mask layer, performing second etching with respect to an entire surface of the insulating film to form, in the insulating film, an opening for exposing the conductive film such that the opening has a diameter larger than a diameter of the depressed portion and a wall surface having a tapered configuration.

28. (Original) The method of claim 27, further comprising the step of:

forming, at least in the opening of the insulating film, a capacitor element composed of a lower electrode, a capacitor insulating film, and an upper electrode.

29. (Original) The method of claim 28, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode;

forming the capacitor insulating film on the lower electrode; and

forming the upper electrode on the capacitor insulating film.

30. (Previously presented) The method of claim 27, further comprising, between the step of forming the mask layer having the first opening pattern and the step of forming the depressed portion in the insulating film, the step of:

forming a wall surface of the first opening pattern into a tapered configuration.

31. (New) The method of claim 14, wherein each of the lower electrode and the upper electrode contains a platinum group element as a main component.

32. (New) The method of claim 14, wherein the capacitor insulating film is composed of a ferroelectric film or a high dielectric film.

33. (New) The method of claim 14, wherein the capacitor insulating film is composed of $SrBi_2(Ta_xNb_{1-x})_2O_9$, $Pb(Zr_xTi_{1-x})O_3$, $(Ba_xSr_{1-x})TiO_3$, $(Bi_xLa_{1-x})_4Ti_3O_{12}$ (where X satisfies a relationship represented by $0 \leq x \leq 1$), or Ta_2O_5.

34. (New) The method of claim 14, wherein the conductive film is composed of iridium, platinum, gold, ruthenium, rhodium, palladium, or a metal oxide thereof or alternatively composed of titanium, titanium-aluminum, tantalum, tantalum-aluminum, a nitride thereof, or a multilayer film composed thereof.

35. (New) The method of claim 14, wherein the conductive film contains an oxygen barrier film.

36. (New) The method of claim 14, wherein the insulating film is an oxide film containing silicon.

37. (New) The method of claim 14, wherein the insulating film has a planarized principal surface.

38. (New) The method of claim 14, wherein the mask layer is a photoresist.

39. (New) The method of claim 12, wherein the conductive film is an oxygen barrier film.

40. (New) The method of claim 39, wherein the oxygen barrier film consists of a titanium-aluminum nitride film, an iridium film, and an iridium oxide film.

41. (New) The method of claim 12, further comprising, before the steps of forming the conductive film, the steps of:

forming a first insulating film on the substrate; and

forming, in the first insulating film, a plug connecting the substrate,

wherein the conductive film is formed on the first insulating film and connecting the plug.